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MARGER JOHNSON & McCOLLOM, P.C.
1030 S.W. Morrison Street
Portland, OR 97205

EXAMINER	
LEE, HSIEN MING	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 05/21/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/043,724	LEE, KANG-YOON	
	Examiner	Art Unit	
	Hsien-Ming Lee	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19 and 21* is/are rejected.

7)☒ Claim(s) *1,3,7,9-14,16,17 and 20-23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement filed 1/8/02 fails to comply with 37 CFR 1.98(a)(1), which requires a list of all patents, publications, or other information submitted for consideration by the Office. The IDS has been placed in the application file, but form 1449 is missing.

Claim Objections

2. Claims 1, 3, 7, 9-14, 16, 17, 20, 21 and 23 are objected to because of the following informalities: in-consistent terminologies. Appropriate correction is required.

Claim 1, at line 4, " each **device**" should be – each area --.

Claim 1, at line 10, " insulating layers" should be – insulating layer --. (see line 10 versus line 12)

Claim 3, at line 21, " first conductivity type transistors" should be -- first conductivity type transistor --. (compare line 21 with line 5)

Claim 7, at line 9, " interlayer insulating layers" should be -- interlayer insulating layer --.

Claim 9, at line 16, " each **device**" should be – each area --.

Claim 10, at line 33 of page 19 and at lines 2 and 5, "**epitaxial** layers" should be – conductive epitaxial layers --.

Claim 11, at line 8, " **the** doping concentration" should be -- a doping concentration --.

Claim 11, at line 8, claim 12 and claim 13, "the **epitaxial** " should be – the conductive epitaxial --.

Claim 14, at line 17, " insulating layers" should be -- insulating layer --.

Claim 16, at line 29, " **the** active area" should be – an active area --.

Claim17, at line 2, "**the** concentration" should be – a concentration --.

Claim 20, at lines 25 and 26, " source/drain **region** " should be -- source/drain regions --.

Claim 21, at line 2 of page 22, " each **device**" should be – each area --.

Claim 23, at line 21, "**the** etch stopping layer" should be either -- the first etch stopping layer – or -- the second etch stopping layer --.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 8 and 21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 8, at lines 26-27, "opening the source/drain regions of the transistors" is unclear to the Examiner because by opening (i.e. cutting) the source/drain regions it would destroy the device. Does it mean -- **forming** openings **in the interlayer insulating layer to expose** the source/drain regions of the transistors --? (Emphasis added)

Claim 21, at lines 9-10 of page 22, "forming openings in the source/drain regions of the transistors" is unclear to the Examiner. Does it mean -- forming openings in the **first insulating layer to expose** the source/drain regions of the transistors --? (Emphasis added)

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 7, 8 and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Yoshida et al. (US 5,981,369).

In re claims 1, 7 and 8, Yoshida et al. expressly teach the claimed method for forming a semiconductor device on a semiconductor substrate, the method comprising:

(a) forming isolation layers 2 that define a memory cell area (i.e. memory array) and a peripheral circuit area on the semiconductor substrate 1 and isolate each area (Figs.1-2);

(b) forming a first conductive type transistor (n-type transistor) 8A in the memory cell area and a first conductive type transistor (n-type transistor) 8B and a second conductive type transistor (p-type transistor) 8C in the peripheral circuit area, each transistor including source/drain regions 11 for 8A, 12/13 for 8B and 14/15 for 8C, a gate electrode, 8A, 8B and 8C having sidewall spacers 10, and a first etch stopping layer 9 (silicon nitride) (Fig.7);

(c) forming an interlayer insulating layer 16 (silicon oxide) overlying the first and second conductive type transistors 8A-8C (Fig.8);

(d) removing portions of the interlayer insulating layer 16 to form openings (i.e. contact holes) 17-22 that expose the source/drain regions 11, 12/13, 14/15 of the transistors 8A-8C in the memory cell area and the peripheral circuit area (Fig.8), and filling the openings 17-22 with a conductive material TiN/W (Fig.9 and col. 5, lines 56-58); and

(e) concurrently forming contact pads (i.e. plug) 23 on the source/drain regions 11 in the memory cell area and the source/drain regions 12/13 and 14/15 in the peripheral circuit area (Fig.9), i.e. comprises etching back the conductive material (i.e. W/TiN) in the memory cell area and the peripheral circuit area, and etching back the interlayer insulating layer 16 in the memory cell area and the peripheral circuit area; and chemical mechanical polishing the conductive material and the interlayer insulating layer 16 as shown in Fig. 9.

In re claim 21, Yoshida et al. expressly teach the claimed method of forming a semiconductor device including a memory cell area having a plurality of memory cells and a peripheral circuit area for writing and reading data in the memory cells in the memory cell area of a semiconductor substrate, the method comprising:

(a) forming isolation layers 2 for defining a memory cell area (i.e. memory array) and a peripheral circuit area on the semiconductor substrate 1 and isolating each area (Figs. 1-2);

(b) forming a first conductive type transistor (n-type) in the memory cell area and a first conductive type transistor and a second conductive type (p-type) transistor in the peripheral circuit area by forming source/drain regions 11, 12/13 and 14/15 and gate electrodes 8A-8C having sidewall spacers 10, and first etch stopping layers 9 (silicon nitride) in the memory cell area and the peripheral circuit area of the semiconductor substrate (Fig.7);

(c) forming a first insulating layer 16 overlying the transistors 8A-8C (Fig.8);

(d) forming plugs (i.e. a layer of tungsten, col.5, lines 56-58) by patterning the insulating layer 16, forming openings 17-22 in the source/drain regions 11, 12/13 and 14/15 of the transistors 8A-8C in the memory cell area and the peripheral circuit area, and filling the openings 17-22 with a conductive material (i.e. tungsten, col.5,lines 56-58);

(e) forming contact pads (i.e. plug) 23 on the source/drain regions 11 in the memory cell area and the source/drain regions 12/13 and 14/15 in the peripheral circuit area (Fig.9), concurrently by etching the first insulating layer 16 and the plugs and then node-separating the plugs;

(f) forming a second insulating layer 27 on the contact pads 23 (Fig.12); and

(g) forming a contact plug 30 on at least one contact pad 23 (Fig.13).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida et al. (US '369) in view of Arima (US 5,949,110).

In re claim 2, Yoshida et al teach all claimed limitation, as stated above, except that the conductive material is doped polysilicon.

However, utilizing the doped polysilicon as conductive material in the application of memory device is a well-known practice, as evidenced by Arima. Arima teaches concurrently forming the doped polysilicon material over a memory cell area and a peripheral circuit area (Fig.3D and col.6, lines 60-67).

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time the invention was made, to utilize the doped polysilicon material as the conductive material as

taught by Arima in the method of Yoshida et al to fill the openings of the interlayer insulating layer, since by this manner it would provide a satisfactory memory cell.

In re claim 3, Yoshida et al in view of Arima also teach the method of claim 2, wherein (d) comprises:

- exposing the source/drain regions 11 and 12/13 of the first conductive type transistors 8A and 8B in the memory cell area and the peripheral circuit area, respectively, by etching the interlayer insulating layer 16 (Fig.8, Yoshida et al);
- forming first conductive type polysilicon layers (i.e. the doped polysilicon of Arima) on the exposed source/drain regions 11 and 12/13 of the first conductive type transistors 8A and 8B, i.e. forming the doped polysilicon material of Arima on the exposed source/drain regions of Yoshida et al;
- exposing the source/drain regions 14/15 of the second conductive type transistor 8C in the peripheral circuit area by etching the interlayer insulating layer 16 (Fig.8 of Yoshida et al); and
- forming a second conductive type polysilicon layer on the exposed source/drain regions 14/15 of the second conductive type transistor 8C, i.e. forming the doped polysilicon as taught by Arima in the openings of the interlayer insulating layer and act as if the plug 23 on the exposed source/drain regions 14/15 of Fig.9 in Yoshida et al.

9. Claims 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida et al. (US '369) in view of Mizutani et al. (US 2002/0014648).

In re claim 4, Yoshida et al. teach gate electrodes 8A-8C have sidewall spacers 10, and first etch stopping layers 9 (silicon nitride) in the memory cell area and the peripheral circuit area of the semiconductor substrate (Fig.7) with the exception of forming a second etch stopping layer overlying the transistors 8A-8C.

However, Mizutani et al. in an analogous art teach forming a second etch stopping layer 25 (silicon nitride) overlying the transistors besides forming a first etch stopping layer 24 (silicon nitride) overlying the transistors (Fig.11F and paragraph [0173]).

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time the invention was made, to form a second etch stopping layer overlying the transistors as taught by Mizutani et al in the method of Yoshida et al., since by this manner two etch stopping layers would form overlying the transistors, which, in turn, would protect the underlying transistors from over-etching during forming the openings in the interlayer insulating layer.

In re clam 5, Yoshida et al in view of Mizutani et al teach that the second etch stopping layer has lower etching selectivity than the interlayer insulating layer because the second etch stopping layer is silicon nitride, whereas the interlayer insulating layer 16 is silicon oxide (col.5, lines 24-26, Yoshida et al.).

In re claim 6, Yoshida et al in view of Mizutani et al teach that the second etch stopping layer is a silicon nitride layer, as stated above.

10. Claims 9-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida et al. (US '369) in view of Nakahata et al. (US 6,417,534).

In re claims 9, 14 and 15, Yoshida et al. teach the claimed method for forming a semiconductor device, comprising:

(a) forming isolation layers 2 for defining a memory cell area and a peripheral circuit area on a semiconductor substrate 1 and isolating each area (Figs. 1-2);

(b) forming a first conductive type transistor (n-type transistor) 8A in the memory cell area and a first conductive type transistor 8B and a second conductive type (p-type transistor) transistor 8C in the peripheral circuit area by forming source/drain regions 11, 12/13 and 14/15 and gate electrodes 8A-8C having sidewall spacers 10, and first etch stopping layer 9 in the memory cell area and the peripheral circuit area of the semiconductor substrate 1 (Fig.7);

(c) forming an interlayer insulating layer 16 overlying the transistors 8A-8C ;

(d) forming plugs (i.e. W/TiN, col. 5, lines 56-58) by patterning the interlayer insulating layer 16, forming openings 17-22 to expose the source/drain regions 11, 12/13 and 14/15 of the transistors 8A-8C in the memory cell area and the peripheral circuit area, and filling the openings 17-22 with metal (W, col.5, lines 56-58); and

(e) concurrently forming metal contact pads 23 in the memory cell area and the peripheral circuit area (Fig.9) by etching back or chemically and mechanically polishing the conductive metal (W/TiN) plugs and the interlayer insulating layer 16.

Yoshida et al. do not teach forming conductive epitaxial layers, which extend from the source/drain regions onto the isolation layers, on the respective source/drain regions; and thus forming an interlayer insulating layer overlying the conductive epitaxial layers.

Nakahata et al. (US 6,417,534) in an analogous art teach forming transistors 8a in memory cell area 1a and transistors 8b and 8c in peripheral area 1b (Fig.5); forming a conductive epitaxial silicon layers 20a and 20b on the bottom of contact holes 18a and 19a (col.22, lines 54-57), which extend from the source/drain regions onto the isolation layers 2a.

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time the invention was made, to form the epitaxial layer extending from the source/drain regions onto the isolation layers as taught by Nakahata et al., in the method of Yoshida et al and forming the interlayer insulating layer overlying the conductive epitaxial layers, since by doing so it would prevent the subsequently formed contact pads from reacting with the source/drain regions and thus reduce current leakage (col.25, lines 20-24, Nakahata et al.).

In re claim10, Yoshida et al in view of Nakahata et al., also inherently teach the limitations because utilizing multiple photoresist patterns as implantation mask for implanting the first and second conductive type impurities on the source/drain regions are necessary steps, as evidenced by Yoshida et al in Figs. 56-58, wherein a photoresist pattern 74 is used for implanting the first conductive type impurities on the source/drain regions (Fig.56) and another photoresist pattern 75 is used for implanting the second conductive type impurities on the source/drain regions (Fig.57).

In re claim 11, the selection of the doping concentration is obvious because it is a matter of determining optimum process condition by routine experimentation with a limited number of species. In re Jones, 162 USPQ 224 (CCPA 1955)(the selection of optimum ranges within prior art general conditions is obvious) and In re Boesch, 205 USPQ 215 (CCPA 1980)(discovery of optimum value of result effective variable in a known process is obvious). For example, the concentration can be selected to sufficiently high to form the doped epitaxial silicon layer that has capability to protect the conductive layer from reacting with source/drain regions. In this case, applicant is required to demonstrate the criticality, generally by showing that the claimed

concentration would achieve unexpected results relative to the prior art. See M.P.E.P. 2144.05 III.

In re claims 12 and 13, Yoshida et al in view of Nakahata et al teach that conductive epitaxial layer comprises silicon (col.22, lines 54-57, Nakahata et al).

11. Claims 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida et al. (US '369) in view of Kauffman et al. (US 6,137,133).

In re claim 16, Yoshida et al. teach the claimed method of forming a semiconductor device having metal contact pads 23 on source/drain regions 8B and 8C of transistors in a peripheral circuit area for writing and reading data in memory cells on a semiconductor substrate, the method comprising:

(a) forming first 8B and second 8C gate electrodes having sidewall spacers 10 and etch stopping layers 9 (silicon nitride) in the peripheral circuit area (Fig. 7);

(b) forming an interlayer insulating layer 16 overlying the first 8B and second 8C gate electrodes;

(c) forming first 8A and 8B (n-type) and second 8C (p-type) conductive type transistors by forming an opening 17-22 in portions of the interlayer insulating layer 16 on an active area including the first 8A and 8B and second 8C gate electrodes, and forming source/drain regions 11, 12/13 and 14/15 (Fig.8);

(d) forming a metal layer (W) in the opening 17-22 (col.5, lines 56-58); and

(e) forming metal contact pads 23 (i.e. plugs) by node-separating the metal layer (Fig.9).

Yoshida et al. do not teach implanting first and second conductive type impurities into the opening of the interlayer insulating layer. Instead, first and second conductive type impurities are implanted before forming the openings (Figs. 5-7).

However, Kauffman et al. in an analogous art of forming memory cell, teach implanting impurities into the openings of the insulating layers 42 (Fig.6) and 54 (Fig.10) to form the source/drain regions 44 and 60 (Fig.10).

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time the invention was made, to implant impurities into the openings of the insulating layers as taught by Kauffman et al, in the method of Yoshida et al to implant the first and second conductive type impurities into the opening of the insulating layer, since by doing so it would simply the processing steps.

In re claim 17, the selection of the concentration of the first and second conductive type impurities is obvious because it is a matter of determining optimum process condition by routine experimentation with a limited number of species. In re Jones, 162 USPQ 224 (CCPA 1955)(the selection of optimum ranges within prior art general conditions is obvious) and In re Boesch, 205 USPQ 215 (CCPA 1980)(discovery of optimum value of result effective variable in a known process is obvious). For example, the concentration can be optimized to form the first and second conductive type transistors that have capability to store input data and perform input and output functions. In this case, applicant is required to demonstrate the criticality, generally by showing that the claimed concentration would achieve unexpected results relative to the prior art. See M.P.E.P. 2144.05 III.

In re claim 18, Yoshida et al. in view of Kauffman et al. also teach (1) forming a first opening (i.e. the opening for plug 23 on the memory cell area) by etching a portion of the interlayer insulating layer 16 on the active area including the first gate electrode 8A; (2) forming a first conductive type source/drain region 11 on the semiconductor substrate 1 by implanting first conductive type impurities (n-type) into the first opening; (3) forming a second opening (i.e. the opening for plug 23 in the peripheral circuit area) by etching a portion of the interlayer insulating layer 16 on the active area including the second gate electrode 8B; and (4) forming a second conductive type source/drain region 14/15 on the semiconductor substrate 1 by implanting second conductive type impurities (p-type) into the second opening adjacent to 8C (Fig.9, Yoshida et al.).

In re claim 19, Yoshida et al. in view of Kauffman et al. also teach (1) etching a portion of the interlayer insulating layer 16 on the active areas each including the first 8A and second gate electrodes 8B; (2) forming a first conductive type source/drain region 11 by implanting first conductive type impurities (n-type) into the active area including the first gate electrode 8A in the first opening (i.e. the opening that exposes region 11); and (3) forming a second conductive type source/drain region 14/15 by implanting second conductive type impurities (p-type) into the second opening (i.e. the opening that exposes region 14/15) (Fig.9, Yoshida et al.)

Allowable Subject Matter

12. Claims 20, 22 and 23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Yoshida et al. to US 5,981,369 teach the claimed method, as stated above, but do not teach or suggest that the insulating layer on a non-active area *between the first and second gate electrodes is removed* so that the source/drain region of the first conductive type transistor is *locally connected* to the source/drain region of the *second* conductive type transistor by the *metal contact pads* which are node-separated (claim 20); and forming a second etch stopping layer on the contact pads (claim 22).

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsien-Ming Lee whose telephone number is 703-305-7341. The examiner can normally be reached on M-F (9:00 ~ 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 703-306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

W David Coleman
Primary Examiner
Art Unit 2823

Hsien Ming Lee
May 14, 2003